Introduction to PMCm

SUMMARY
Programmable Metallization Cell memory (PMCm) represents a radical departure from all existing memory technologies, including those currently in development. PMCm utilizes solid state electrochemistry to attain easily detectable non-volatile changes in a simple, highly scalable structure at hitherto unattainably low voltage and energy. PMCm is a solution to the memory scaling quandary which has the ability to take us beyond the 30 nm node on the International Technology Roadmap for Semiconductors (ITRS).

BACKGROUND
In recent years, a field of science called Solid State Ionics has received increasing attention. Similar to the way in which the behavior of electrons in semiconductors has been exploited to create solid-state electronics and ultimately the microelectronics industry, ion mobility and the associated electrochemical phenomena in solid-state materials form the basis for revolutionary products and perhaps entirely new industries. When combined with the mature technologies developed over the last fifty years in the semiconductor world, the result is a discipline which we call *integrated ionics*. Integrated ionic devices have desirable electrical, optical, mechanical, and chemical attributes which are limited or unavailable in purely electronic systems.

Axon Technologies Corporation is a technology creation and licensing company. It was founded in 1996 to develop and commercialize its revolutionary and proprietary technology, the Programmable Metallization Cell (PMC), a cornerstone of Integrated Ionics. PMC technology has applications in such diverse fields as microelectronics, optoelectronics, and microfluidics, but it is the applications relating to solid-state *memory* that have generated the highest level of commercial interest to date.

TIMING
The introduction of PMCm technology comes at a very opportune time in computer system development. Although we have a roadmap (the ITRS) that can be reasonably expected to lead to a steady reduction in transistor size over the next decade, its translation into new products and markets faces some serious obstacles. Productivity in circuit design lags that in manufacturing so although we may be able to make chips with billions of logic transistors in 2014, limited design resources will restrict us to much more modest capabilities. One solution is to add more memory and reuse existing logic designs. This is an effective and pragmatic approach but it shifts the constraint to memory circuits.

Both of today's mainstream memory technologies – DRAM for core memory and flash for non-volatile embedded memory – are running out of steam. In the case of flash, the problems arise from the steady reduction in supply voltages when device programmability rests on a high voltage, quasi-breakdown process. DRAM technology needs new dielectric materials to allow adequate charge to be stored in the small areas of future devices. Neither technology faces an abrupt cut-off, but unless viable

alternatives are developed, performance will fall steadily behind the full roadmap potential and the historical trend of continuous reduction in cost per bit will end. Newer memory technologies such as FeRAM and MRAM face even greater materials issues than DRAM and the experience of the semiconductor industry has been that such problems take longer than expected to solve.

Against this background of impending limits in conventional technology, PMCm offers simplicity of concept leading to efficient manufacturing and the applications flexibility that will come from having one high-density memory cell that can be used for both dynamic and non-volatile applications.

SCIENTIFIC BASIS

Certain solid materials will allow the movement of metal ions under the influence of an electric field – these are generally referred to as *solid electrolytes*. If electrodes are formed in contact with a layer of solid electrolyte, an anode which has an oxidizable form of the metal in solution and an inert cathode, an ion current will flow as long as the applied bias is in excess of the oxidation potential for the metal, typically a few hundred mV, and as long as there is oxidizable silver at the positive electrode. The electron current flow from the cathode will cause the reduction of the metal ions and hence a metal-rich electrodeposit will be formed on or in the electrolyte. The amount of electrodeposited material (metal in excess of the starting composition of the electrolyte) is determined by the ion current magnitude and the time it is allowed to flow. The process is reversible by applying a reverse bias so that the electrodeposited metal is now the oxidizable “anode”. The reverse ion current will flow until the previously electrodeposited material has been oxidized and deposited back on the electrode which originally supplied the excess metal. This ability to electrically increase and subsequently decrease the metal content of the solid electrolyte, and thereby significantly change an electrical parameter associated with the structure, is the basis of the PMCm technology.

KEY ATTRIBUTES

The key attributes of a high density solid state memory are:

(1) low internal voltage to allow the close packing of structures without breakdown and crosstalk and to reduce power supply requirements,
(2) extremely low power/energy consumption to avoid problems with power density and heating in closely-packed structures and to facilitate the use of small battery power sources in portable applications, and
(3) the ability for the devices to be scaled to minimum lithographic dimensions.

PMCm readily meets these requirements with sub-0.3 volt write and erase, microamp range programming current, and speed in the ten nanosecond regime, combined with physical scalability to the nanoscale.

MANUFACTURING

One of the strongest features of PMCm technology is the extent to which it is totally compatible with anticipated developments in conventional integrated circuit manufacturing. Logic, I/O, sense and switching circuits can all be fabricated in silicon and the PMCm cells added as part of the interconnect matrix on top. The electrodes and electrolyte thin films are typically deposited by PVD, using standard semiconductor processing equipment. Since the typical PMCm device resides in a via and is formed during back end of line (BEOL) activities, nitride barrier materials such as those used in copper interconnect processing may be used as liners and seals.

The format of a PMCm fabrication plant will be very similar to a conventional wafer fab. Wafer size, automation, fab tools, measurement, control and facilities will all be familiar. This is the strongest indicator that introduction, value propositions and customer support can be built on realistic and achievable projections.

PROPOSED POINT OF INTRODUCTION

Existing memory technologies such as DRAM and Flash will doubtless be hard to displace from the non-embedded “pure memory” sector of the marketplace. However, many technologists agree that major problems relating to desired price-performance characteristics of existing memory types will begin to surface around the 90 nm node on the International Technology Roadmap for Semiconductors (ITRS) in 2004. The proposed point of introduction of PMCm technology is therefore at the 90 nm node although it could, of course, be sooner if applications or economics dictate.

TECHNOLOGY LONGEVITY

Looking forward 12 years, the International Technology Roadmap for Semiconductors (ITRS) in its section on Process Integration, Devices, and Structures gives goals for long term memory technology requirements at the 2014 or 30 nm node, to which we have added current and projected PMC capability.

Parameter	**ITRS**	**PMCm**
Minimum V_{dd} (V)	0.3 - 0.6	0.25 (1)
DRAM cell size (μm^2)	0.0031	<0.0018 (2)
DRAM retention time (msec)	250 - 500	>500
Non-volatile retention (years)	0.1 - 10	>0.1
NVM endurance (cycles)	10^5 - 10^7	>10^{13}

Notes:
(1) Normal write and erase are both performed between 0.2 and 0.3 V.
(2) The cell area given for PMC is based on a single $(2F)^2$ cell with double bit storage.